

HALL TICKET NUMBER

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PACE INSTITUTE OF TECHNOLOGY & SCIENCES::ONGOLE  
(AUTONOMOUS)

II B.TECH I SEMESTER END SUPPLEMENTARY EXAMINATIONS, JAN - 2023  
DIGITAL LOGIC DESIGN

(Common to CSE, CSE(IOTCSBT) Branches)

Time: 3 hours

Max. Marks: 60

Note: Question Paper consists of Two parts (Part-A and Part-B)

PART-A

Answer all the questions in Part-A (5X2=10M)

Q.No.	Questions	Marks	CO	KL
1	a) Convert $(2469)_{10}$ in to BCD.	[2M]	1	
	b) State De-Morgan's Theorems.	[2M]	2	
	c) What are advantages of tabulation method over k-map. Draw the K map for 5 variables.	[2M]	3	
	d) Implement the function $F = \sum m(1, 2, 3, 7)$ using 3:8 decoder.	[2M]	4	
	e) Distinguish between latch and flip-flop.	[2M]	5	

PART-B

Answer One Question from each UNIT (5X10=50M)

Q.No.	Questions	Marks	CO	KL
UNIT-I				
2.	a) Interpret the following to Decimal and then to Binary i) $(ABCD)_{16}$ ii) $(7234)_8$	[5M]	1	
	b) Deduce i) $(231)_{10} - (37)_{10}$ using BCD numbers with 10's complement method ii) $(13)_{10} - (159)_{10}$ using Excess-3 codes with 9's complement method	[5M]	1	
OR				
3.	a) A receiver with even parity hamming code receives the data 1110110. Determine the correct code.	[5M]	1	
	b) What is the gray code? What are the rules to construct gray code? Develop the 4-bit gray code for the decimal 0 to 15.	[5M]	1	
UNIT-II				
4.	a) Implement AND,NOT,OR,NOR logic gates using NAND gate	[5M]	2	
	b) Obtain the Dual of the following Boolean expressions a) $AB + A(B+C) + B'(B+D)$ b) $A+B+A'B'C$	[5M]	2	
OR				
5.	a) Obtain the Dual of the following Boolean expressions a) $A'B + A'BC' + A'BC'D'E$ b) $ABEF + ABE'F' + A'B'EF$	[5M]	2	
	b) Express the function $AB'D + AC'D + A'BD$ in sum of minterms and product of maxterms.	[5M]	2	
UNIT-III				
6.	a) Simplify the given Boolean function using K-map $F = \sum m(0,2,3,4,6,7,8,11,12,13)$	[5M]	3	
	b) Simplify the expression $F = \sum m(4,5,9,13,15) + d(0,1,7,11,12)$ using K-map and realize using logic gates.	[5M]	3	
OR				

7.	a)	What do you mean by K-map? Name its advantages and disadvantages.	[5M]	3	
	b)	Obtain minimal POS expression for the given function and implement it in NOR logic. $f = \pi M(2,4,5,6,8,10,12,13,14,15)$	[5M]	3	
UNIT-IV					
8.	a)	Design the full subtractor and give its applications.	[5M]	4	
	b)	Design 16x1 Multiplexer using two 4x1 Multiplexers	[5M]	4	
OR					
9.	a)	What is decoder? Construct 3 X 8 decoder using logic gates and truth table.	[5M]	4	
	b)	Write about combinational logic circuit for BCD adder.	[5M]	4	
UNIT-V					
10.	a)	Compare synchronous & Asynchronous circuits.	[5M]	5	
	b)	Build the circuit of JK flip-flop using NAND gates and explain its operation with the help of its characteristic table.	[5M]	5	
OR					
11.	a)	Draw the circuit of D flip-flop using NOR gates and explain its operation with the help of its characteristic table.	[5M]	5	
	b)	Design a Mod-6 synchronous counter using J-K flip flops.	[5M]	5	

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